Changes to the Claims

Claim 1 (Cancelled).

2. (Original) A method for fabricating integrated circuits of the type having first cells and a first conductor disposed in a first plane, and at least second cells and a second conductor disposed in at least a second plane substantially parallel to the first plane, said method comprising the steps of:

a) forming a vertical interconnection disposed for connecting said first conductor with said second conductor, said vertical interconnection extending at least between said first and second planes and initially including an antifuse, and

b) subsequently fusing said antifuse to form a continuous electrical connection for electrically coupling said first conductor with at least said second conductor.

3. (Original) An integrated circuit fabricated by the method of claim 2.

Claims 4-18 (Cancelled).

19. (Original) A method for fabricating integrated circuits, comprising the steps of:

a) disposing first cells and a first conductor in a first plane,

b) disposing at least second cells and a second conductor in at least a second plane substantially parallel to the first plane,

c) forming a vertical interconnection disposed for connecting said first conductor with said second conductor, said vertical interconnection extending at least between said first and second planes and initially including an antifuse, and

d) subsequently fusing said antifuse to form a continuous electrical connection for electrically coupling said first conductor with at least said second conductor.

20. (Original) An integrated circuit fabricated by the method of claim 19.

21. (Original) The method of claim 19, wherein said vertical-interconnection forming step (c) is performed by a sub-method comprising the steps of:

i) disposing a suitable thin oxide upon said first conductor, and

ii) disposing a conductive via material upon said suitable thin oxide whereby a tunnel-junction antifuse is formed.

22. (Original) The method of claim 19, wherein said antifuse-fusing step (d) is performed by applying a voltage and current sufficient to form a continuous electrical connection.

23. (Original) The method of claim 19, wherein said antifuse-fusing step (d) is performed by applying a current through a conductor redundant to normal operation of said integrated circuits.

24. (Original) The method of claim 19, wherein said antifuse-fusing step (d) is performed by applying a current through a diode.

25. (Original) A method for fabricating integrated circuits, comprising the steps of:

a) forming and disposing first cells and a first conductor in a first plane,

b) forming and disposing at least second cells and a second conductor in at least a second plane substantially parallel to the first plane,

c) forming a vertical interconnection disposed for connecting said first conductor with said second conductor, said vertical interconnection extending at least between said first and second planes and initially including an antifuse, said antifuse being formed by substeps comprising:

i) disposing a suitable thin oxide upon said first conductor, and

ii) disposing a conductive via material upon said suitable thin oxide whereby a tunnel-junction antifuse is formed, and

d) subsequently fusing said antifuse by applying a voltage and current sufficient to form a continuous electrical connection for electrically coupling said first conductor with at least said second conductor.

26. (Original) An integrated circuit fabricated by the method of claim 25.

27. (Original) The method of claim 25, wherein said antifuse-fusing step (d) is performed by applying a current through a conductor redundant to normal operation of said integrated circuits.

28. (Original) An integrated circuit fabricated by the method of claim 27.

29. (Orignal) The method of claim 25, wherein said antifuse-fusing step (d) is performed by applying a current through a diode.

30. (Orignal) An integrated circuit fabricated by the method of claim 29.

Claims 31-53 (Cancelled).

54. (Original) A method for fabricating integrated circuits, said method comprising the steps of:

a) disposing first cells and a first conductor in a first plane,

b) providing a multiplicity of row conductors and a multiplicity of column conductors,

c) disposing at least second cells and a second conductor in at least a second plane substantially parallel to the first plane, at least one of said first and second conductors being coupled to one of said multiplicity of row conductors,

d) forming a vertical interconnection disposed for connecting said first conductor with said second conductor, said vertical interconnection extending at least between said first and second planes and initially including an antifuse, and

e) subsequently fusing said antifuse to form a continuous electrical connection for electrically coupling said first conductor with at least said second conductor by activating said one of said multiplicity of row conductors and all of said multiplicity of column conductors.

55. (Original) An integrated circuit fabricated by the method of claim 54.

56. (Original) The method of claim 54, further comprising selectively repeating said fusing step (e) for each selected row conductor of said multiplicity of row conductors.

57. (Original) An integrated circuit fabricated by the method of claim 56.

58. (Original) A method for fabricating integrated circuits, said method comprising the steps of:

a) disposing first cells and a first conductor in a first plane,

b) providing a multiplicity of row conductors and a multiplicity of column conductors,

c) disposing at least second cells and a second conductor in at least a second plane substantially parallel to the first plane, at least one of said first and second conductors being coupled to one of said multiplicity of column conductors,

d) forming a vertical interconnection disposed for connecting said first conductor with said second conductor, said vertical interconnection extending at least between said first and second planes and initially including an antifuse, and

e) subsequently fusing said antifuse to form a continuous electrical connection for electrically coupling said first conductor with at least said second conductor by activating said one of said multiplicity of column conductors and all of said multiplicity of row conductors.

59. (Original) An integrated circuit fabricated by the method of claim 58.

60. (Original) The method of claim 58, further comprising selectively repeating said fusing step (e) for each selected column conductor of said multiplicity of column conductors.

61. (Original) An integrated circuit fabricated by the method of claim 60.

62. (Original) A method for fabricating integrated circuits, comprising the steps of:

a) disposing first cells and a first conductor in a first plane,

b) providing at least one redundant row conductor and at least one redundant column conductor,

c) disposing at least second cells and a second conductor in at least a second plane substantially parallel to the first plane,

d) forming a vertical interconnection disposed for connecting said first conductor with said second conductor, said vertical interconnection extending at least between said first and second planes and initially including an antifuse, and

e) subsequently fusing said antifuse by supplying to at least one of said at least one redundant row conductor and said at least one redundant column conductor sufficient voltage and current to form a continuous electrical connection for electrically coupling said first conductor with at least said second conductor.

63. (Original) An integrated circuit fabricated by the method of claim 62.

64. (Original) The method of claim 62, further comprising selectively repeating said fusing step (e) for each selected vertical interconnection.

65. (Original) An integrated circuit fabricated by the method of claim 64.

66. (Original) The method of claim 62, wherein said first and second cells are each disposed in arrays having array edges, further comprising the step of disposing said at least one redundant row conductor and at least one redundant column conductor adjacent to said array edges of said arrays.

67. (Original) An integrated circuit fabricated by the method of claim 66.